RTL8103T

Integrated Fast Ethernet Controller for PCI Express™ Applications

General Description

This product is covered by one or more of the following patents:
US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

The Realtek RTL8103T-GR Fast Ethernet controller combines an IEEE 100/10 802.3Base-T compliant Media Access Controller (MAC), PCI Express bus controller, and embedded One-Time-Programmable (OTP) memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8103T offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 100/10Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8103T features embedded One-Time-Programmable (OTP) memory to replace the external EEPROM (93C46).

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™ and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8103T.

The RTL8103T is fully compliant with Microsoft® NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8103T supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. The device embeds an adaptive equalizer in the PCIE PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 20 inches.

The RTL8103T is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

Built-in linear regulators provide the RTL8103T's core power, as well as reducing layout area and external BOM costs. The RTL8103T supports the Deep Slumber Mode (DSM) power saving feature. See the separate DSM application notes for details.

Features

Integrated 100/10 transceiver
Auto-Negotiation with Next Page capability
Supports PCI Express™ 1.1
Supports pair swap/polarity/skew correction
Crossover Detection & Auto-Correction
Wake-on-LAN and remote wake-up support
Customizable LEDs
Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
Supports Full Duplex flow control (IEEE 802.3x)
Fully complies with IEEE 802.3, IEEE 802.3u
Supports IEEE 802.1P Layer 2 Priority Encoding
Supports IEEE 802.1Q VLAN tagging
Serial EEPROM
Embedded OTP memory can replace the external EEPROM
Transmit/Receive on-chip buffer support
Supports power down/link down power saving
Built-in Regulator
Supports PCI MSI (Message Signaled Interrupt) and MSI-X
Supports Receive-Side Scaling (RSS)
Embeds an adaptive equalizer in PCI express PHY (PCB traces can reach up to 20 inches)
Supports Deep Slumber Mode (DSM) power saving feature
-32pin QFN Green package

Applications

PCI Express™ Fast Ethernet on Motherboard, Notebook, or Embedded system